CLAIMS AS AMENDED

1. (Currently Amended) A memory cell, comprising two gated ~~lateral~~ vertically stacked bipolar transistors ~~and having~~ configured to exhibit two bistable current states for storing information, one of said current states being achieved by operation of gate-induced latchup of said transistors.

2. (Currently Amended) The memory cell of claim 1 wherein said gated ~~lateral~~ vertically stacked bipolar transistors comprise two complementary vertical bipolar transistors.

3. (Currently Amended) The memory cell of claim 2 wherein said complementary bipolar transistors comprise a p-n-p transistor and an n-p-n transistor ~~and the collector region of~~ , said p-n-p transistor ~~is connected with the base region of~~ and said n-p-n transistor sharing their central n- and p-regions.

4. (Currently Amended) The memory cell of claim 3 wherein said p-n-p transistor ~~further~~ comprises a first gate ~~in connection with~~ spanning the central n-region of said p-n-p transistor.

5. (Currently Amended) The memory cell of claim 4 wherein said n-p-n transistor ~~further~~ comprises a second gate ~~in connection with~~ spanning the p-region of said n-p-n transistor.

6. (Currently Amended) The memory cell of claim 5 wherein said gate-induced latchup ~~is achieved by a pulsed gate bias~~ is effected by turning on both said first and second gates.

7. (Currently Amended) The memory cell of claim 6 wherein said ~~pulsed gate bias biases the gate in connection with one of the n-region or the p-region and~~

~~subsequently biases the gate in connection with the other of the n-region or p-region~~ first and second gates are orthogonally positioned relative to each other.

8. (Original) The memory cell of claim 1 wherein said cell is a static random access memory cell.

9. (Original) The memory cell of claim 1 wherein said cell has an area of about $4F^2$ where F is the minimum lithographic dimension.

10. (Currently Amended) A circuit for storing information as one of at least two possible bistable current states, comprising at least one vertical p-n-p-n structure containing a bipolar p-n-p transistor merged with a bipolar n-p-n transistor at central n- and p-regions of said structure;

a first transistor gate ~~in connection with~~ spanning the central n-region of said p-n-p transistor; and

a second transistor gate ~~in connection with~~ spanning the central p-region of said n-p-n transistor.

11. (Currently Amended) The circuit of claim 10 wherein said transistor gates ~~operate~~ are configured to latch-up said p-n-p-n structure ~~and~~ , wherein said latch-up results in one of said bistable current states.

12. (Currently Amended) The memory cell of claim 11 wherein said ~~pulsed gate bias biases the gate in connection with one of the n-region or the p-region and subsequently biases the gate in connection with the other of the n-region or p-region~~ latch-up results in said memory cell having a lowered resistance.

13. (Original) The circuit of claim 11 further comprising a substrate for supporting said vertical p-n-p-n structure.

14. (Original) The circuit of claim 12 wherein said vertical p-n-p-n structure is disposed in a trench within said substrate.

15. (Original) The circuit of claim 11 wherein said circuit is a static random access memory cell.

16. (Original) The circuit of claim 14 wherein said memory cell has an area of about $4F^2$ where F is the minimum lithographic dimension.

17. (Currently Amended) A SRAM cell, comprising:

a ~~p-n-p-n~~ vertical transistor stack having a first p-region, a first n-region, a second p-region, and a second n-region; and

a first gate ~~in connection with~~ bridging said first and second p-regions across the first n-region, and a second gate ~~in connection with~~ bridging said first and second n-regions across said second p-region, wherein said first and second gates are ~~connected to at least one voltage source for producing~~ configured to produce latch-up in said ~~p-n-p-n~~ vertical transistor stack as ~~one of the bistable~~ a current ~~states~~ state for storing information in said SRAM cell.

18. (Currently Amended) The SRAM cell of claim 17 wherein said latch-up is produced by providing a ~~pulsed gate bias~~ voltage pulse in both said first and second gates.

19. (Currently Amended) The memory cell of claim 18 wherein said ~~pulsed gate bias biases the gate in connection with one of the first n-region or the second p-region and subsequently biases the gate in connection with the other of the first n-region or second p-region~~ first and second gates are positioned orthogonally to each other.

20. (Original) The SRAM cell of claim 17 further comprising a substrate for supporting said p-n-p-n transistor and wherein said p-n-p-n transistor is a vertical structure disposed within a trench in said substrate.

21. (Currently Amended) The SRAM cell of claim 17 further comprising a row address line ~~in connection~~ electrically coupled with the first p-region and a column address line ~~in connection~~ electrically coupled with the second n-region.

22. (Currently Amended) The SRAM cell of claim 21 further comprising a write row address line ~~in connection~~ electrically coupled with said first gate ~~connecting to said first n-region,~~ and a column write address line ~~in connection~~ electrically coupled with said second gate ~~connecting to said second p-region~~.

23. (Currently Amended) A SRAM array, comprising

a substrate;

a plurality of vertical ~~p-n-p-n~~ transistors, each of said transistors being merged p-n-p and n-p-n transistors;

a first set of isolation trenches between said ~~p-n-p-n~~ vertical transistors for isolating said vertical transistors in a first direction;

a second set of isolation trenches orthogonal to said first set of trenches for isolating said vertical transistors in a second direction;

a first gate line in at least some ~~of said~~ trenches of said first set of isolation trenches ~~and~~ , said first gate line connecting ~~the~~ central n-regions of at least some of said ~~plurality of~~ vertical transistors; and

a second gate line in at least some of said trenches of said second set of isolation trenches ~~and~~ , said second gate line connecting ~~the~~ central p-regions of at least some of said ~~plurality of~~ vertical transistors.

24. (Currently Amended) The SRAM array of claim 23 further comprising an insulating material layer between each of said ~~p-n-p-n~~ vertical transistors and the substrate, ~~horizontally~~ thereby at least partially isolating the vertical transistors.

25. (Original) The SRAM array of claim 24 wherein said insulating material is an oxide.

26. (Original) The SRAM array of claim 24 wherein said insulating material is a buried n-type layer.

27. (Currently Amended) The SRAM array of claim 23 wherein said plurality of ~~p-n-p-n~~ vertical transistors are inverted ~~transistors~~ and are supported ~~on~~ by a p-type substrate.

28. (Original) A computer system, comprising

a processor; and

a memory circuit connected to the processor, the memory circuit containing at least one memory cell comprising two gated complementary bipolar transistors and having bistable current states for storing information, one of said current states being achieved by operation of gate-induced latch-up of said transistors, wherein the complementary bipolar transistors comprise a vertical p-n-p transistor and a vertical n-p-n transistor and the collector region of said p-n-p transistor is connected with the base region of said n-p-n transistor.

29. (Currently Amended) The computer system of claim 33 wherein said p-n-p transistor has a first gate ~~in connection with~~ spanning the n-region of said p-n-p transistor, and said n-p-n transistor has a second gate ~~in connection with~~ spanning the p-region of said n-p-n transistor.

30. (Currently Amended) The computer system of claim 28 wherein said gate-induced latchup is achieved by ~~a pulsed gate bias~~ turning on both first and second gates.

31. (Currently Amended) The computer system of claim 30 wherein said ~~pulsed gate bias biases the gate in connection with one of the n-region or the p-region and subsequently biases the gate in connection with the other of the n-region or p-region~~ first and second gates are positioned adjacent to said transistors and orthogonal to each other.

32. (Original) The computer system of claim 28 wherein said memory cell is a static random access memory cell.

33. (Original) The computer system of claim 32 wherein said static random access memory cell has an area of about $4F^2$ where F is the minimum lithographic dimension.

34-54 (Cancelled)